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| Substitute for form 1449A/PTO | | Complete if Known Application Number: 10/710,596 Filing Date: July 23, 2004 First Named Inventor: MOU-SHIUNG LIN Art Unit: 2811 Examiner Name: COLLEEN ANN MATTHEWS | |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i> | | | |
| Sheet | 1 | of | 3 |
| Attorney Docket No: 085027-0101 | | | |

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| Examiner Initial * | Cite No | Document Number | Publication Date | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
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| | 1 | MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250 | |
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